K5/VSSP (IP-VLBI) Board Data Format

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1 Introduction

The K5/VSSP (IP-VLBI) board is capable to sample either 1 channel or 4 channels of analog input with one of the quantization levels of 1 bit, 2 bits, 4 bits, or 8 bits. Sampling frequency can be set from 40kHz, 100kHz, 200kHz, 500kHz, 1MHz, 2MHz, 4MHz, 8MHz, or 16MHz. Sampled data can be stored to a data file on an internal hard disk drive. In addition, the data can be sent to the network interface by using UDP/IP or TCP/IP. In the following section, the data format of the data file created by the IP VLBI board is described.

2 Data structure

A data file contains sampled data for certain amount of time obtained by one IP VLBI board. The data file begins with a header section (HD) of the length of 64 bits and then 1 second of data stream is written in the sampling data section (SD) following the header section. This sequence repeats until the scan of the observation finishes as shown in the Table 1. The data format of each data section is described in the following subsections.

Header section (HD)	Sampling data section (SD)	HD	· ·
64 bits	40000 - 64000000 bits	64 bits	· ·

Figure 1: Data structure of the data file

2.1 Header section data format

A header section consists of 32 bits of HD1 and 32 bits of HD2. In the HD1 section, all bits are 1. In the HD2 section, time stamp and sampling information are written with the format explained in the Table 2.

2.2 Sampling data section

Data format of the sampling data section is described with the first 64 bits in the Tables 3 through 10.

Table 1: Data format of the header section

HD1 (32bits)

D0	(LSB)	Sync pattern (32 bits)
:		[FF FF FF FF]
D31	(MSB)	

HD2 (32 bits)

D0	(LSB)	Time (time of day) (17 bits)
:		(0〜86399 sec)
D16		elapsed time from 00h00m00s in seconds
D17		Index of the number of channels 0:1ch 1:4ch
D18		Index of sampling frequency (4 bits)
:		(Note: definitions for more than a 32MHz sampling are to support
:		the conversion from other format data such as Mark5)
:		0: 40kHz / 1: 100kHz / 2: 200kHz / 3: 500kHz
:		4: 1MHz / 5: 2MHz /6: 4MHz / 7: 8MHz / 8: 16MHz
:		9: 32MHz / 10: 64MHz / 11: 128MHz / 12: 256MHz / 13: 512MHz
D21		14: 1024MHz / 15: 2048MHz
D22		Index of the number of quantization (2 bits)
D23		0: 1 bit / 1: 2 bits / 2: 4 bits / 3: 8 bits
D24		Sync pattern 2 (8 bits)
:		[8Bh]
D31	(MSB)	

Table 2: Sampling data section data format (1 ch / 1 bit sampling)

1 ch / 1 bit sampling		
1st 32bits data		
D0	(LSB)	1st data (1bit)
D1		2nd data (1bit)
:		:
D31	(MSB)	32nd data (1bit)
2nd 32bits data		
D0	(LSB)	33rd data (1bit)
D1		34th data (1bit)
:		:
D31	(MSB)	64th data (1bit)
:		

Table 3: Sampling data section data format (1 ch / 2 bits sampling)

1 ch / 2 bits sampling		
1st 32bits data		
D0	(LSB)	1st data (2bits LSB)
D1		1st data (2bits MSB)
D2		2nd data (2bits LSB)
D3		2nd data (2bits MSB
:		:
D31	(MSB)	16th data (2bits MSB)
2nd 32bits data		
D0	(LSB)	17th data (2bits LSB)
D1		17th data (2bits MSB)
D2		18th data (2bits LSB)
D3		18th data (2bits MSB)
:		:
D31	(MSB)	32th data (2bits MSB)
:		

Table 4: Sampling data section data format (1 ch / 4 bits sampling)

1 st / 4 bits sampling		
1st 32bits data		
D0	(LSB)	1st data (4bits LSB)
:		:
D3		1st data (4bits MSB)
D4		2nd data (4bits LSB)
:		:
D7		2nd data (4bits MSB)
:		:
D31		8th data (4bits MSB)
2nd 32bits data		
D0	(LSB)	9th data (4bits LSB)
:		:
D31		16th data (4bits MSB)
:		

Table 5: Sampling data section data format (1 ch / 8 bits sampling)

1 ch / 8 bits sampling		
1st 32bits data		
D0	(LSB)	1st data (8bits LSB)
:		:
D7		1st data (8bits MSB)
D8		2nd data (8bits LSB)
:		:
D15		2nd data (8bits MSB)
:		:
D31		4th data (8bits MSB)
2nd 32bits data		
D0	(LSB)	5th data (8bits LSB)
:		:
D31		8th data (8bits MSB)
:		

Table 6: Sampling data section data format (4 ch / 1 bit sampling)

4 ch / 1 bit sampling		
1st 32bits data		
D0	(LSB)	Ch.1 1st data (1bit)
D1		Ch.2 1st data (1bit)
D2		Ch.3 1st data (1bit)
D3		Ch.4 1st data (1bit)
D4		Ch.1 2nd data (1bit)
D5		Ch.2 2nd data (1bit)
:		:
D31	(MSB)	Ch.4 8th data (1bit)
2nd 32bits data		
D0	(LSB)	Ch.1 9th data (1bit)
D1		Ch.2 9th data (1bit)
:		:
D31	(MSB)	Ch.4 16th data (1bit)
:		

Table 7: Sampling data section data format (4 ch / 2 bits sampling)

4 ch / 2 bits sampling		
1st 32bits data		
D0	(LSB)	Ch.1 1st data (2bits LSB)
D1		Ch.1 1st data (2bits MSB)
D2		Ch.2 1st data (2bits LSB)
D3		Ch.2 1st data (2bits MSB)
D4		Ch.3 1st data (2bits LSB)
D5		Ch.3 1st data (2bits MSB)
D6		Ch.4 1st data (2bits LSB)
D7		Ch.4 1st data (2bits MSB)
D8		Ch.1 2nd data (2bits LSB)
D9		Ch.1 2nd data (2bits MSB)
:		:
D31	(MSB)	Ch.4 4th data (2bits MSB)
2nd 32bits data		
D0	(LSB)	Ch.1 5th data (2bits LSB)
D1		Ch.1 5th data (2bits MSB)
D2		Ch.2 5th data (2bits LSB)
D3		Ch.2 5th data (2bits MSB)
:		:
D31	(MSB)	Ch.4 8th data (2bits MSB)
:		

Table 8: Sampling data section data format (4 ch / 4 bits sampling)

4 ch / 4 bits sampling		
1st 32bits data		
D0	(LSB)	Ch.1 1st data (4bits LSB)
:		:
D3		Ch.1 1st data (4bits MSB)
D4		Ch.2 1st data (4bits LSB)
:		:
D7		Ch.2 1st data (4bits MSB)
D8		Ch.3 1st data (4bits LSB)
:		:
D11		Ch.3 1st data (4bits MSB)
D12		Ch.4 1st data (4bits LSB)
:		:
D15		Ch.4 1st data (4bits MSB)
D16		Ch.1 2nd data (4bits LSB)
:		:
D19		Ch.1 2nd data (4bits MSB)
:		:
D31		Ch.4 2nd data (4bits MSB)
2nd 32bits data		
D0	(LSB)	Ch.1 3rd data (4bits LSB)
:		:
D31		Ch.4 4th data (4bits MSB)
:		

Table 9: Sampling data section data format (4 ch / 8 bits sampling)

4 ch / 8 bits sampling		
1st 32bits data		
D0	(LSB)	Ch.1 1st data (8bits LSB)
:		:
D7		Ch.1 1st data (8bits MSB)
D8		Ch.2 1st data (8bits LSB)
:		:
D15		Ch.2 1st data (8bits MSB)
D16		Ch.3 1st data (8bits LSB)
:		:
D23		Ch.3 1st data (8bits MSB)
D24		Ch.4 1st data (8bits LSB)
:		:
D31		Ch.4 1st data (8bits MSB)
2nd 32bits data		
D0	(LSB)	Ch.1 2nd data (8bits LSB)
:		:
D31		Ch.4 2nd data (8bits MSB)
:		